WHAT IS CLAIMED IS:

1. A DRAM apparatus, comprising:

a storage cell including a transistor having a substrate well; and

a voltage adjuster coupled to said substrate well for adjusting a voltage on said substrate well.

2. The apparatus of Claim 1, including an input coupled to said storage cell for accessing said storage cell, said voltage adjuster coupled to said input and responsive to activation of said input for adjusting the voltage on said substrate well.

3. The apparatus of Claim 2, wherein said input is a wordline.

4. The apparatus of Claim 2, wherein said voltage adjuster includes a switch coupled to said input and said substrate well, said switch responsive to activation of said input for initiating adjustment of the voltage on said substrate well.

5. The apparatus of Claim 4, wherein said voltage adjuster includes a node at a predetermined voltage coupled to said switch.

6. The apparatus of Claim 5, wherein said node is coupled to said substrate well.

7. The apparatus of Claim 5, wherein said voltage adjuster includes a resistor connected in series between said switch and said node.

8. The apparatus of Claim 7, wherein said switch includes a transistor, said transistor having a gate coupled to said input, a drain coupled to said resistor and said substrate well, and a source coupled to a voltage source.

9. The apparatus of Claim 5, wherein said voltage adjuster includes a further node at a further predetermined voltage coupled to said switch.

10. The apparatus of Claim 9, wherein said voltage adjuster includes a resistor connected in series between said first-mentioned node and said switch, said switch responsive to activation of said input for connecting said resistor to said further node, said substrate well connected to said resistor.

11. The apparatus of Claim 10, wherein said first-mentioned voltage is approximately –0.5 volts and said further voltage is approximately 0 volts.

12. The apparatus of Claim 1, including a plurality of said storage cells having said substrate wells thereof connected together and also connected to said voltage adjuster.

13. An apparatus for controlling access to a data storage element in a memory device, comprising:

a transistor for accessing said data storage element, said transistor including a substrate well; and

a circuit coupled to said substrate well for adjusting a voltage on said substrate well.

14. The apparatus of Claim 13, including an input coupled to said transistor for controlling access to said data storage element, said circuit coupled to said input and responsive to activation of said input for adjusting the voltage on said substrate well.

15. The apparatus of Claim 14, wherein said circuit includes a switch coupled to said input and said substrate well, said switch responsive to activation of said input for initiating adjustment of the voltage on said substrate well.

16. The apparatus of Claim 15, wherein said circuit includes a node at a predetermined voltage coupled to said switch.

17. The apparatus of Claim 16, wherein said circuit includes a further node at a further predetermined voltage coupled to said switch.

18. The apparatus of Claim 17, wherein said circuit includes a resistor connected in series between said first-mentioned node and said switch, said switch responsive to activation of said input for connecting said resistor to said further node, said substrate well connected to said resistor.

19. The apparatus of Claim 13, wherein said data storage element includes a capacitor.

20. A method of accessing a data storage capacitor in a memory device, the method comprising:

activating a node of a transistor used to access said data storage element; and

adjusting a voltage on a substrate well of said transistor in response to said activating step.

21. The method of Claim 20, wherein said activating step includes activating a gate of the transistor.